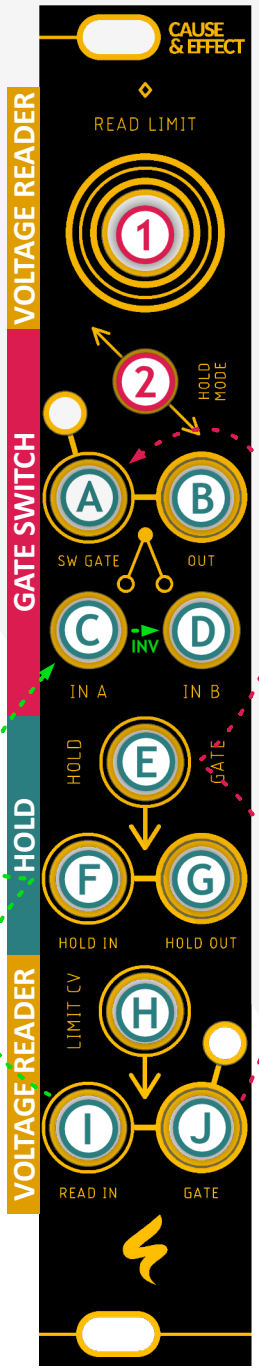
CAUSE & EFFECT **QUICK START** GUIDE



VOLTAGE READER (COMPARATOR)
outputs a gate signal corresponding to a limit value set using the READ LIMIT potentiometer. The limit value can be controlled via voltage.

GATE SWITCH (A/B SWITCH)
If a gate signal is applied to the SW GATE input only IN B will be connected to the output jack. If gate is low IN A is available at the output.

HOLD (SAMPLE/TRACK & HOLD)
In one mode, it samples and stores a voltage from the HOLD IN jack, supplying it at the HOLD OUT jack when the gate at H GATE is high (sample & hold). In another mode, it passes through the incoming voltage when the gate is high and stores the last applied voltage value when the gate switches to low (track & hold).

CONTROLS

1. **READ LIMIT** of the voltage reader controls the threshold value at which the incoming CV triggers a gate signal at the gate output **(J)**.

2. Toggle between sample & hold and track & hold modes of the HOLD function block by adjusting the **HOLD MODE** switch.

INPUTS & OUTPUTS

A. SW GATE switch input**.** Apply a gate signal here to route IN A **(C)** or IN B **(D)** to OUT **(B)**. If the gate signal is high, IN A is switched through, and if the gate signal is low, IN B is switched through. When only IN A is connected and IN B is not, OUT produces an inverted version of IN A when the gate is low, and a non-inverted version when high. When only IN B is connected and IN A patched with a dummy cable, IN B can be switched off by a gate signal. If nothing is patched to IN A, the VOLTAGE READER GATE output **(J)** is normalized to this input.

B. OUT gate switch output that outputs either IN A **(C)** or IN B **(D)** depending on the state of SW GATE **(A)**.

C + D. Gate switch inputs **IN A and IN B.** Apply any voltage to these inputs, one of which is connected to the output **(B)** depending on the state of SW GATE **(A)**. If nothing is connected to IN B **(D)**, an inverted copy of IN A **(C)** is normalised to this input. If nothing is connected to IN A **(C)**, the READ IN **(I)** input of the VOLTAGE READER is normalised to this input.

E. HOLD GATE. A patched gate signal determines when the input is sampled and constantly routed to the HOLD OUT **(G)** socket. If nothing is patched here, the VOLTAGE READER GATE output **(J)** is normalized to this input.

F. The **HOLD IN** input receives a control voltage that can be sampled, tracked or held by the HOLD function block. The READ IN **(I)** input of the VOLTAGE READER is standardised to this input if it is not patched.

G. Use the **HOLD OUT** output to pick up the sampled or tracked signal from the HOLD function block.

H. The **LIMIT CV** voltage reader CV input enables the control of the voltage reader's threshold value using a control voltage. If a cable is patched, the READ LIMIT potentiometer **(1)** serves as an offset control.

I. READ IN voltage reader input. Receives voltage, compares it to the threshold, and produces a high or low gate output accordingly.

J. GATE voltage reader output. Outputs a gate of +/-5V depending on the READ IN **(I)** input and the READ LIMIT control **(1)**. This output is able to generate square waves with pulse width modulation via the READ LIMIT knob **(1).**

OTHER

- Accepted input voltages for all inputs: -8V to +8V (AC & DC).
- Calibration is not required.
- This guide applies equally to the 3U and 1U versions.
- Use the VOLTAGE READER to control all other blocks via internal normalisations (shown with arrows in the illustration).